FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. APLUS.001A	APPLICATION NO. 09/754,406
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	APPLICANT Songjie Xu	RECEIVED
	FILING DATE January 2, 2001	GROUP 2123

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
MCH	1.	Singh, K.J., Performance Optimization of Digital Circuits, Ph.D. Dissertation, pages 33-79, University of California at Berkeley, 1992
MCH	2.	Pan, P., Performance-Driven Integration of Retiming and Resynthesis, in Proc. Design Automation Conf., pages 243-246, 1999
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MCH	4.	Sentovich et al., SIS: A System for Sequential Circuit Synthesis, Electronics Research Laboratory, Memorandum No. UCB/ERL M92/41, 1992
MCH	5.	Hwang, Y.-Y.. Logic Synthesis for Lookup-Table Based Field Programmable Gate Arrays, Ph.D. Dissertation, pages 35-63, University of California at Los Angeles, 1999
MCH	6.	Yang, S., Logic Synthesis and Optimization Benchmarks User Guide Version 3.0, Technique Report, MCNC, January 1991

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EXAMINER Mary C. Hogan	DATE CONSIDERED 5/13/04

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.